The language objected to was intended to convey the fact that the debugger (44 in Figure 2) runs on its own clock and the processor (10 in Figure 2) runs on its own clock. Therefore, the debugger can, according to the invention, determine whether a debugger clock cycle has occurred without the processor executing an instruction. What is really meant by this is that the debugger can determine whether the processor has stalled. According to the invention, the debugger indicates every time the processor stalls that the processor has stalled as now provided for in amended claim 21.

Claims 21, 24, and 25 stand rejected under 35 U.S.C. §103(a) as obvious over Segars et al. in view of Ueki. The Examiner relies on Segars et al. for teaching indicating when the processor has stalled. Column 13 of Seagars et al. indicates that a processor stall is indicated when executing a branch instruction. However, there is no suggestion that an indication be provided every time the processor stalls regardless of cause. The present invention indicates whenever the processor stalls and is thus capable of debugging pipeline errors which the prior art cannot debug.

As claims 24 and 25 depend from claim 21, the argument made above applies to these claims as well.

In light of all of the above, it is submitted that all of the claims are in order for allowance, and prompt allowance is earnestly requested. Should any issues remain outstanding, the Examiner is invited to call the undersigned attorney of record so that the case may proceed expeditiously to allowance.

Respectfully submitted,

David P. Gordon

David P. Gordon
Reg. #29,996
Attorney for Applicant(s)

65 Woods End Road
Stamford, CT 06905
(203) 329-1160

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